REMARKS

In the Office Action dated September 21, 2004, claims 1-18 and 31-60 were pending. Claims 1-10, 11-13, 14-15, 16-18, and 31-60 were rejected under 35 U.S.C. § 103(a).

In this response, no claim has been cancelled. Claims 1, 4, 7, 10-11, 13, and 16 have been amended. No new matter has been added. Reconsideration of this application as amended is respectfully requested.

Claims 1-10, 14-15, 31-60 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bashford, U.S. Patent No. 6,629,179 ("Bashford") in view of Pawlowski, U.S. Patent No. 5,956,516 ("Pawlowski"). Claims 11-13 and 16-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bashford, in view of Pawlowski, and further in view of Tyner, U.S. Patent No. 6,564,276 ("Tyner").

In view of the foregoing amendments, it is respectfully submitted that 1-18 and 31-60 include limitations that are not disclosed or suggested by the cited references, individually or in combination. Specifically, independent claim 1 recites as follows:

> 1. A method comprising:
> receiving at an IO controller hub an interrupt from an IO device;
> the IO controller hub converting said interrupt into an upstream memory write interrupt by generating a memory write request to a predetermined address of a memory space, the memory write request being processed via one or more memory cycles by a memory controller hub; and
> the memory controller hub converting said upstream memory write interrupt into a front side bus (FSB) interrupt transaction, wherein one or more processors coupled to the FSB are capable of receiving the FSB interrupt as a part of a FSB transaction.

(Emphasis added)

Independent claim 1 includes a limitation of an IO controller receiving an interrupt from an IO device and converting the interrupt into an upstream memory write interrupt by

generating a memory request at a predetermined address processed by a memory controller. The memory controller then converts the memory write interrupt into a processor bus interrupt. It is respectfully submitted that these limitations are absent from the cited references, individually or in combination.

Rather, Bashford is related to a PCI-PCI bridge that processes interrupts between different PCI buses. Although Bashford discloses a message signed interrupt (MSI), such MSI is intended to be used by a PCI-PCI bridge (e.g., a "south" bridge as recognized in the art). The transactions of Bashford are not performed within a chipset or a "north" bridge of a system.

In contrast, the present invention as claimed is related to interrupt conversion within a chipset or a "north" bridge having an IO controller and a memory controller, where the IO controller converts an IO interrupt into a memory write interrupt which is routed to the memory controller. The memory controller then converts the memory write interrupt into a processor bus (also referred to as front-side bus or FSB) interrupt.

In the Office Action, the Examiner contends that sections of col. 1, line 60 to col. 2, line 20 and col. 5, line 30 to col. 6, line 22 of Bashford disclose an IO controller generating a memory write interrupt at a predetermined address and a memory controller processes the memory write interrupt (see, page 3 of the Office Action). Applicant respectfully disagrees.

The cited sections of Bashford are related to PCI bus transactions. As described above, Bashford is related to a PCI-PCI bridge (e.g., a south bridge), where none of the IO controller and memory controller (which are located within the chipset or the north bridge) is involved. An IO controller and a memory controller have specific meanings in the art and they normally located within a chipset or a north bridge. Specifically, Bashford fails to disclose an IO controller (of a chipset or north bridge) converting an IO interrupt into a

memory write interrupt and a memory controller converting the memory write interrupt into a processor bus interrupt.

Although Pawlowski discloses routing an interrupt to a processor bus, however, Pawlowski still fails to disclose converting an IO interrupt into a memory write interrupt and then converting the memory write interrupt into a processor bus interrupt. Specifically, Pawlowski fails to disclose an IO controller convert an IO interrupt into a memory write interrupt and a memory controller converting the memory write interrupt into a processor bus interrupt. Tyner also fails to disclose or suggest the limitations set forth above.

In addition, there is no suggestion within Bashford and Pawlowski to combine with each other. As discussed above, Bashford is related to a PCI-PCI bridge, which is considered as a "south" bridge, while Pawlowski is related to a host bridge, which is considered as a "north" bridge. The north bridge typically is part of a chipset coupling a processor bus to a system bus. The south bridge is typically used to couple other PCI buses to the system bus. The designs of these two bridges are significantly different and their functionalities are significantly different. It is respectfully submitted that one with ordinary skill in the art would not combine Bashford with Pawlowski, because it lacks motivation and reasonable expectation of success.

Even if they were combined, such a combination still lacks the limitations set forth above. Therefore, for the reasons discussed above, it is respectfully submitted that independent claim 1 is patentable over Bashford in view of Pawlowski.

Similarly, independent claims 4, 7, 10, 31, 34, 37, 44, 51, 59 include limitations similar to those recited in claim 1. Thus, for the reasons similar to those discussed above, it is respectfully submitted that claims 4, 7, 10, 31, 34, 37, 44, 51, 59 are patentable over Bashford in view of Pawlowski.

Given that the reset of the claims depend from one of the above independent claims, it is respectfully submitted that the rest of the claims are patentable over Bashford in view of Pawlowski. Withdrawal of the rejections is respectfully requested.

Furthermore, in the Office Action, the Examiner stated that certain claims of the present application fail to include the terms of FSB (front-side bus) discussed in the previous arguments (see, page 7 of the Office Action). It is respectfully submitted that the terms of a front-side bus and a processor bus are interchangeable terms in the art.

In view of the foregoing, Applicants respectfully submit the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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